X67BC7321-1

1 General information

This X67 bus controller makes it possible to connect X2X Link I/O nodes to CAN I/O. CAN I/O is a transfer protocol based on standard CAN bus that is fully integrated in the B&R system. From the user's point of view, it does not matter if I/O points are operated locally or remotely via CAN I/O.

The CAN I/O bus controller is supported by CAN I/O master versions beginning with CANIO library V1.20.4. Up to 43 logical I/O modules can be connected to the bus controller. Up to 16 can be analog modules.

- Fieldbus: CAN bus
- 8 digital channels, configurable as inputs or outputs
- Integrated I/O access in B&R Automation Studio
- Automatic firmware update via the fieldbus
- X67 connection possibility for all B&R CPUs

Information:

The bus controller is unable to detect modules after a gap in the X2X Link station numbers. This can result from the following:

- **Unconnected X67 modules**
- **Modules with integrated node number switches**

Information:

This bus controller only supports the standard function model for multi-function modules. The standard function model is explained in the description for each multi-function module.

2 Order data

Model number	Short description	Figure
	Bus controller modules	
X67BC7321-1	X67 bus controller, 1 CAN I/O interface, extended CAN I/O function, X2X Link power supply 3 W, 8 digital channels configurable as inputs or outputs, 24 VDC, 0.5 A, configurable input filter, 2 event counters 50 kHz	

Table 1: X67BC7321-1 - Order data

Required accessories
See "Required cables and connectors" on page 6.

3 Technical data

Model number	X67BC7321-1
Short description	
Bus controller	CAN I/O
General information	
Inputs/Outputs	8 digital channels, configurable as inputs or outputs using software, inputs with additional functions
Isolation voltage between channel and bus	500 V_{Eff}
Nominal voltage	24 VDC
B&R ID code	
Bus controller	0x18CB
Internal I/O module	0x1311
Sensor/Actuator power supply	0.5 A summation current
Status indicators	I/O function for each channel, supply voltage, bus function
Diagnostics	
Outputs	Yes, using status LED and software
I/O power supply	Yes, using status LED and software
Connection type	
Fieldbus	M12, A-keyed
X2X Link	M12, B-keyed
Inputs/Outputs	8x M8, 3-pin
I/O power supply	M8, 4-pin
Power output	3 W X2X Link power supply for I/O modules
Power consumption	
Fieldbus	2.1 W
Internal I/O	2 W
X2X Link power supply	6.2 W at maximum power output for connected I/O modules
Electrical isolation	
Fieldbus - X2X Link	No
Channel - Bus	Yes (CAN bus and X2X Link)
Channel - Channel	No
Certification	
CE	Yes
KC	Yes
UL	cULus E115267 Industrial Control Equipment
HazLoc	cCSAus 244665 Process Control Equipment for Hazardous Locations Class I, Division 2, Groups ABCD, T5
ATEX	Zone 2, II 3G Ex nA IIA T5 Gc IP67, Ta = 0 - max. 60°C TÜV 05 ATEX 7201X
GOST-R	Yes
Interfaces	
Fieldbus	CAN I/O
Design	M12 interface (male connector on the module)
Max. distance	1000 m
Transfer rate	Max. 1 Mbit/s
Default transfer rate	Automatic transfer rate detection
Min. cycle time [1]	
Fieldbus	1 ms
X2X Link	1 ms
Synchronization between bus systems possible	No
Terminating resistor	Can be optionally screwed onto the Y-connector
I/O power supply	
Nominal voltage	24 VDC
Voltage range	18 to 30 VDC
Integrated protection	Reverse polarity protection
Power consumption	
Sensor/Actuator power supply	Max. 12 W [2]
Sensor/Actuator power supply	
Voltage	Module power supply minus voltage drop for short circuit protection
Voltage drop for short circuit protection at 0.5 A	Max. 2 VDC
Summation current	Max. 0.5 A
Short circuit protection	Yes
Digital inputs	
Input voltage	18 to 30 VDC
Input current at 24 VDC	Typ. 4 mA
Input filter	
Hardware	≤10 µs (channels 1 to 4) / ≤70 µs (channels 5 to 8)
Software	Default 0 ms, configurable between 0 and 25 ms in 0.2 ms intervals
Input circuit	Sink
Additional functions	50 kHz event counting, gate measurement

Table 2: X67BC7321-1 - Technical data

Model number	X67BC7321-1
Input resistance	Typ. 6 kΩ
Switching threshold	
Low	<5 VDC
High	>15 VDC
Event counter	
Quantity	2
Signal form	Square wave pulse
Evaluation	Each falling edge, cyclic counter
Input frequency	Max. 50 kHz
Counter 1	Input 1
Counter 2	Input 3
Counter frequency	Max. 50 kHz
Counter size	16-bit
Gate measurement	
Quantity	1
Signal form	Square wave pulse
Evaluation	Rising edge - Falling edge
Counter frequency	
Internal	48 MHz, 3 MHz, 187.5 kHz
Counter size	16-bit
Length of pause between pulses	≥100 µs
Pulse length	≥20 µs
Supported inputs	Input 2 or input 4
Digital outputs	
Design	FET positive switching
Switching voltage	Module power supply minus residual voltage
Nominal output current	0.5 A
Total nominal current	4 A
Output circuit	Source
Output protection	Thermal cutoff for overcurrent and short circuit, integrated protection for switching inductances, reverse polarity protection for output power supply
Diagnostic status	Output monitoring with 10 ms delay
Leakage current when switched off	5 µA
Switching on after overload cutoff	Approx. 10 ms (depends on the module temperature)
Residual voltage	<0.3 V at 0.5 A rated current
Peak short circuit current	<12 A
Switching delay	
0 -> 1	<400 µs
1 -> 0	<400 µs
Switching frequency	
Resistive load	Max. 100 Hz
Inductive load	See section "Switching inductive loads"
Braking voltage when switching off inductive loads	50 VDC
Operating conditions	
Mounting orientation	
Any	Yes
Installation at elevations above sea level	
0 to 2000 m	No limitations
>2000 m	Reduction of ambient temperature by 0.5°C per 100 m
EN 60529 protection	IP67
Environmental conditions	
Temperature	
Operation	-25 to 60°C
Derating	-
Storage	-40 to 85°C
Transport	-40 to 85°C
Mechanical characteristics	
Dimensions	
Width	53 mm
Height	85 mm
Depth	42 mm
Weight	195 g
Torque for connections	
M8	Max. 0.4 Nm
M12	Max. 0.6 Nm

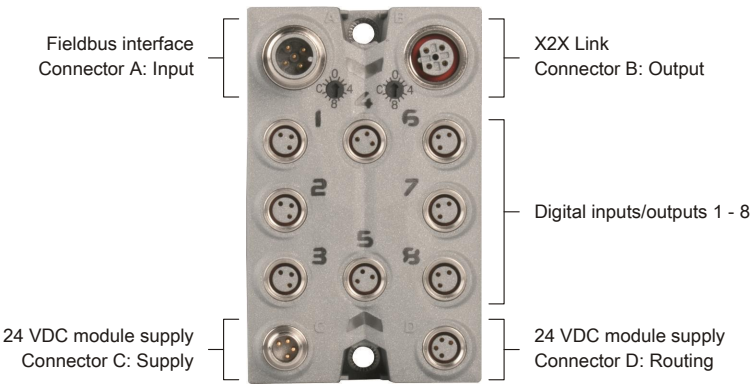
Table 2: X67BC7321-1 - Technical data

1) The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring.
2) The power consumption of the sensors and actuators connected to the module is not permitted to exceed 12 W.

4 LED status indicators

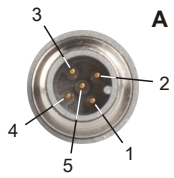
Figure	LED	Color	Status	Description
	**Status indicator 1**			
	Left	Status indicator for CAN I/O bus controller		
		Green	Off	No power supply via CAN fieldbus
			Flickering	Transfer rate detection in progress
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	Right	Status indicator for the CAN fieldbus		
		Red	Off	No power supply via CAN fieldbus or everything OK
			Flickering	Transfer rate detection in progress
			Single flash	CAN connection reporting "Warning limit reached"
			On	CAN connection reporting "BusOff state"
	I/O LEDs			
	1 - 8	Orange	-	Input/Output status of the corresponding channel
	Status indicator 2: Status indicator for module function			
	Left	Green	Off	No power to module
			Single flash	RESET mode
			Blinking	PREOPERATIONAL mode
			On	RUN mode
	Right	Red	Off	No power to module or everything OK
			On	Error or reset status
			Single flash	Warning/Error on an I/O channel. Level monitoring for digital outputs has been triggered.
			Double flash	Supply voltage not in the valid range

5 Operating and connection elements



6 Fieldbus interface

The bus controller is connected to the fieldbus using pre-assembled cables. The connection is made using M12 circular connectors.

Connection	Pinout	
	**Pin**	**Name**
	1	Shield[1)]
	2	Not used
	3	CAN⊥
	4	CAN_High
	5	CAN_Low
	1) Shield connection also made via threaded insert in the module A → A-keyed (male), input	

6.1 Node number and transfer rate

The node number and transfer rate are configured using the two number switches on the bus controller. The switch positions 0x00 to 0x40 and 0x60 enable automatic transfer rate detection (see section "Automatic transfer rate detection" on page 5). The rest of the switch positions have a fixed transfer rate (see table).

Switch position	Node number	Transfer rate
0x00[1)]	From EEPROM	From EEPROM
0x01 - 0x3F	1 - 63	Automatic
0x40[1)]	From EEPROM	From EEPROM
0x41 - 0x5F	1 - 31	1000 kbit/s
0x60[1)]	From EEPROM	From EEPROM
0x61 - 0x7F	1 - 31	800 kbit/s
0x80	Reserved	-
0x81 - 0x9F	1 - 31	500 kbit/s
0xA0	Reserved	-
0xA1 - 0xBF	1 - 31	250 kbit/s
0xC0	Reserved	-
0xC1 - 0xDF	1 - 31	125 kbit/s
0xE0	Reserved	-
0xE1 - 0xFE	1 - 31	20 kbit/s
0xFF	Reserved	-

1) When one of these numbers is configured, the bus controller uses the operating parameters from the internal EEPROM. The EEPROM is programmed using library CANIO.

6.1.1 Automatic transfer rate detection

After booting, the bus controller goes into "Listen only" mode. This means the bus controller behaves passively on the bus and only listens.

The bus controller attempts to receive valid objects. If receive errors occur, the controller switches to the next transfer rate in the lookup table.

If no objects are received, all transfer rates are tested cyclically. This procedure is repeated until valid objects are received.

Starting transfer rate

The bus controller begins the search with this transfer rate. The starting transfer rate can be defined in two different ways:

- Read from EEPROM
- Using the last detected transfer rate after a software reset (command code 20)

Lookup table

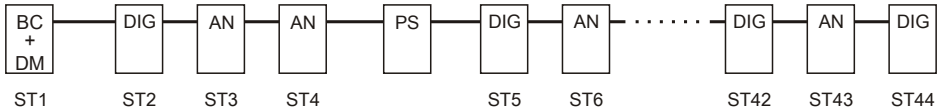
The controller tests the transfer rate according to this table. Beginning with the starting transfer rate, the controller switches to the next lower transfer rate. At the end of the table, the bus controller restarts the search from the beginning.

Transfer rate
1000 kbit/s
500 kbit/s
250 kbit/s
125 kbit/s
50 kbit/s
20 kbit/s
10 kbit/s

6.2 System configuration

The X67DM1321 digital mixed module is already integrated in the bus controller. This makes the bus controller the first I/O module on the CAN bus (ST1 → Station 1).

Up to 28 logical digital modules (including bus controller) and 16 logical analog modules can be operated on the bus controller. There is no fixed order of modules. Digital and analog modules can be arranged as needed.



Key:
BC → Bus controller
DM → Digital mixed module
DIG → Digital module
AN → Analog module
ST → Station
PS → Power supply module X67PS1300 (not counted as a station on the CAN bus)

Information:

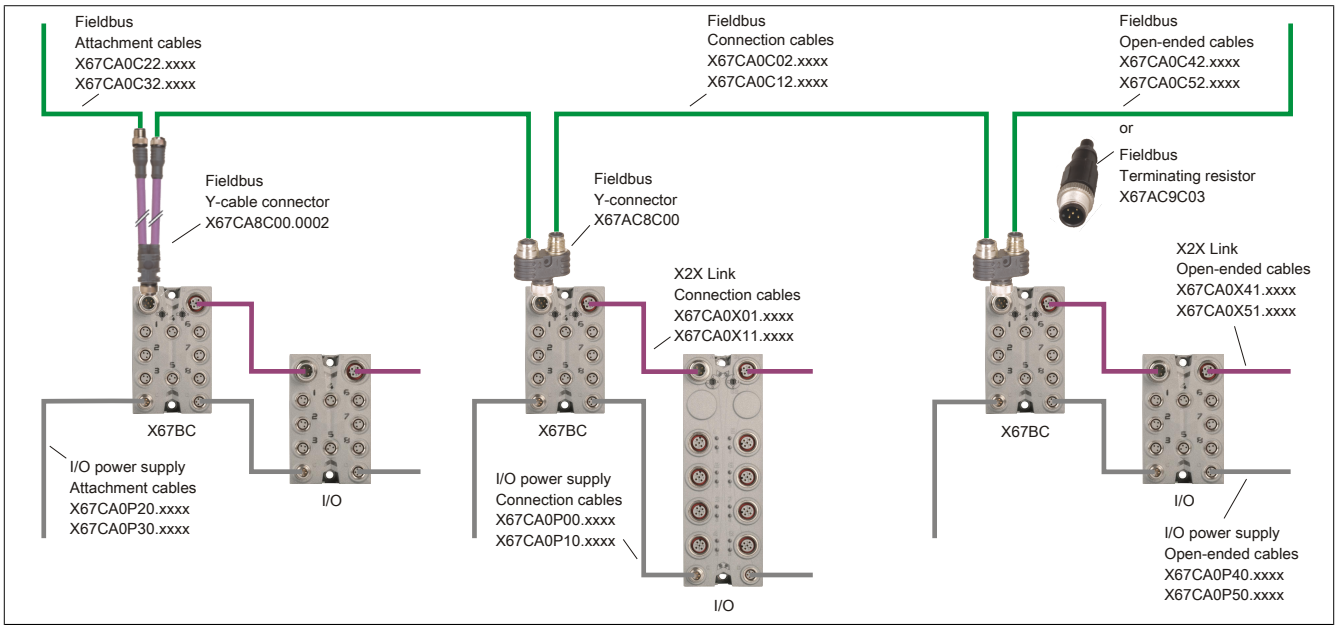
3 W are provided by the bus controller for additional X67 modules or other X2X Link-based modules.

Power supply module X67PS1300 is needed for additional power. This power supply module provides 15 W for additional modules. It should be mounted in the middle of the modules that are to be supplied with power.

6.3 Required cables and connectors

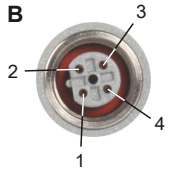
The bus controller is connected to the fieldbus using a Y-connector. This allows the bus controller to be exchanged without interrupting fieldbus communication.

The bus terminating resistor is housed in a connector and screwed onto the Y-connector when needed.



7 X2X Link

Additional modules are connected to the bus controller via X2X Link using pre-assembled cables. The connection is made using M12 circular connectors.

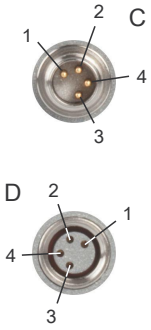
Connection	Pinout	
	**Pin**	**Name**
	1	X2X+
	2	X2X
	3	X2X⊥
	4	X2X\
	Shield provided by threaded insert in the module	
	B → B-keyed (female), output	

8 Module power supply 24 VDC

The module supply is connected via M8 connectors C and D. The power supply is connected via connection C (male). Connector D (female) is used to route the power supply to other modules.

Information:

The maximum permitted current for the module power supply is 8 A (4 A per pin).

Connection	Pinout		
	**Pin**	**Connector C (male)**	**Connector D (female)**
	1	24 VDC fieldbus	24 VDC module
	2	24 VDC module	24 VDC I/O
	3	GND	GND
	4	GND	GND
	C → Connector (male) in module, feed for module power supply D → Connector (female) in module, routing of module power supply		

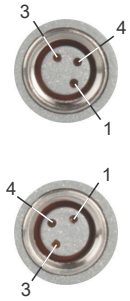
9 Integrated digital mixed module

1 additional mixed module can be saved by the digital mixed module integrated in the bus controller.

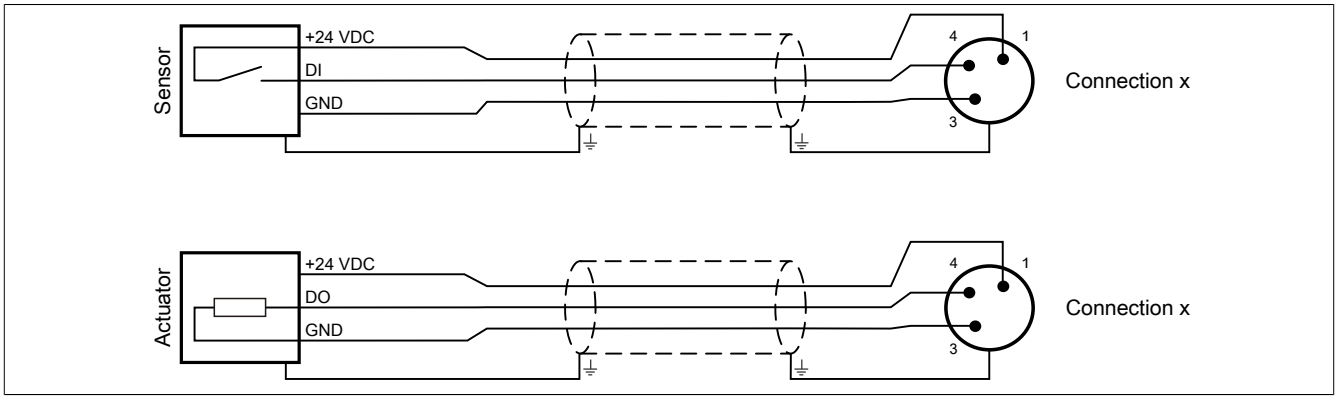
9.1 Pinout

① X67CA0D40.xxxx: M8 straight sensor cable
X67CA0D50.xxxx: M8 angled sensor cable

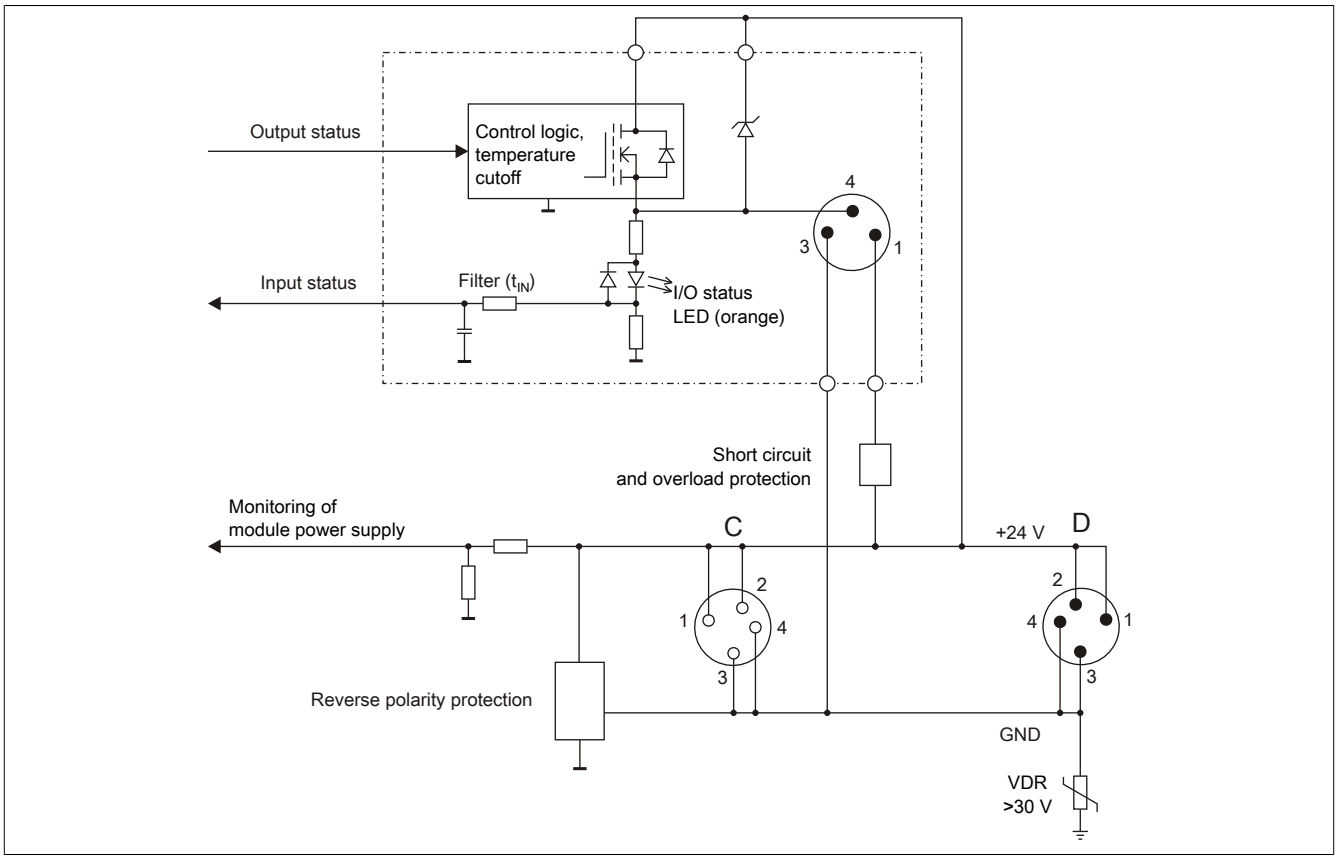
9.2 Connection X1 to X8

M8, 3-pin	Pinout	
	**Pin**	**Name**
	1	24 VDC sensor/actuator power supply[1)]
	3	GND
	4	Inputs/Outputs
	Shield connection made via threaded insert in the module. 1) Sensors/Actuators are not permitted to be supplied externally. Connections (female), input/output	

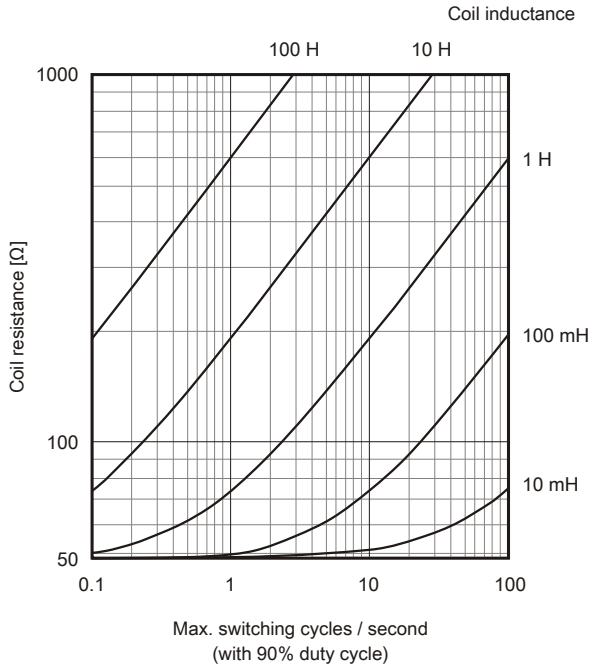
9.3 Connection example



9.4 Input/Output circuit diagram



9.5 Switching inductive loads



10 SG4

This module comes with preinstalled firmware. The firmware is also part of the Automation Runtime operating system for the PLC. If the two versions are different, the Automation Runtime firmware is loaded to the module.

The latest firmware is made available automatically when updating Automation Runtime.

11 Logical I/O modules

Up to 43 I/O modules can be connected to the bus controller (up to 16 can be analog modules). This value refers not to the physical but the logical I/O module slots.

Information:

Physical I/O modules can take up more than one digital or analog slot.

The following table lists all X67 modules capable of using CAN bus and how many logical digital and analog slots are needed.

Module	Digital module slots	Analog module slots
X67AI1223	0	1
X67AI1233	0	1
X67AI1323	0	1
X67AI1333	0	1
X67AI2744	0	**2**
X67AI4850	0	1
X67AM1223	0	1
X67AM1323	0	1
X67AO1223	0	1
X67AO1323	0	1
X67AT1311	0	1
X67AT1322	0	1
X67AT1402	0	1
X67BC7321-1	1	0
X67DC1198	0	**2**
X67DC2322	0	**2**
X67DI1371	1	0
X67DI1371.L08	**2**	0
X67DI1371.L12	**2**	0
X67DI1372	1	0
X67DM1321	1	0
X67DM1321.L08	**2**	0
X67DM1321.L12-1	**2**	0
X67DM1321.L12	**2**	0
X67DM9321	1	0
X67DM9321.L12	**2**	0
X67DM9331.L12	1	0
X67DO1332	1	0
X67DO9332.L12	1	0
X67DV1311.L08	**2**	0
X67DV1311.L12	**2**	0
X67IF1121-1	0	**3**
X67MM2436	0	**2**
X67SM2436	0	**2**
X67SM4320	0	**4**
X67UM4389	0	**2**

12 Register description

12.1 General data points

In addition to the registers listed in the register description, the module also has other more general data points. These registers are not specific to the module but contain general information such as serial number and hardware version.

These general data points are listed in section "Additional information - General data points" of the X67 system user's manual.

12.2 Function model 2 - Standard

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
16	ConfigIOMask01	USINT				•
18	ConfigOutput03 (input filter)	USINT				•
Communication						
0	Input state of digital inputs 1 to 8	USINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput08	Bit 7				
2	Switching state of digital outputs 1 to 8	USINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput08	Bit 7				
30	Status of digital outputs 1 to 8	USINT	•			
	StatusDigitalOutput01	Bit 0				
	...	...				
	StatusDigitalOutput08	Bit 7				
26	Input latch - Rising edges 1 to 8	USINT	•			
	InputLatch01	Bit 0				
	...	...				
	InputLatch08	Bit 7				
28	Acknowledgment - Input latch 1 to 8	USINT			•	
	QuitInputLatch01	Bit 0				
	...	...				
	QuitInputLatch08	Bit 7				
8192	asy_ModulID	UINT		•		
8196	asy_SupplyStatus	USINT		•		
8208	asy_SupplyInput	USINT		•		

12.3 Function model 1 - Counter

Register	Name	Data type	Read		Write	
			Cyclic	Acyclic	Cyclic	Acyclic
Configuration						
16	ConfigIOMask01	USINT				•
20	ConfigOutput01 (counter channel 1)	USINT				•
22	ConfigOutput02 (counter channel 2)	USINT				•
18	ConfigOutput03 (input filter)	USINT				•
Communication						
0	Input state of digital inputs 1 to 8	USINT	•			
	DigitalInput01	Bit 0				
	...	...				
	DigitalInput08	Bit 7				
2	Switching state of digital outputs 1 to 8	USINT			•	
	DigitalOutput01	Bit 0				
	...	...				
	DigitalOutput08	Bit 7				
30	Status of digital outputs 1 to 8	USINT	•			
	StatusDigitalOutput01	Bit 0				
	...	...				
	StatusDigitalOutput08	Bit 7				
26	Input latch - Rising edges 1 to 8	USINT	•			
	InputLatch01	Bit 0				
	...	...				
	InputLatch08	Bit 7				
28	Acknowledgment - Input latch 1 to 8	USINT			•	
	QuitInputLatch01	Bit 0				
	...	...				
	QuitInputLatch08	Bit 7				
4	Counter01	UINT	•			
6	Counter02	UINT	•			
20	Reset counter 1	USINT			•	
	ResetCounter01	Bit 5				
22	Reset counter 2	USINT			•	
	ResetCounter02	Bit 5				
8192	asy_ModulID	UINT		•		
8196	asy_SupplyStatus	USINT		•		
8208	asy_SupplyInput	USINT		•		

12.4 Function model 254 - Bus controller

Register	Offset[1)]	Name	Data type	Read		Write	
				Cyclic	Acyclic	Cyclic	Acyclic
Configuration							
16	-	ConfigIOMask01	USINT				•
20	-	ConfigOutput01 (counter channel 1)	USINT				•
22	-	ConfigOutput02 (counter channel 2)	USINT				•
18	-	ConfigOutput03 (input filter)	USINT				•
Communication							
0	0	Input state of digital inputs 1 to 8	USINT	•			
		DigitalInput01	Bit 0				
		...	...				
		DigitalInput08	Bit 7				
2	0	Switching state of digital outputs 1 to 8	USINT			•	
		DigitalOutput01	Bit 0				
		...	...				
		DigitalOutput08	Bit 7				
30	-	Status of digital outputs 1 to 8	USINT	•			
		StatusDigitalOutput01	Bit 0				
		...	...				
		StatusDigitalOutput08	Bit 7				
26	-	Input latch - Rising edges 1 to 8	USINT	•			
		InputLatch01	Bit 0				
		...	...				
		InputLatch08	Bit 7				
28	-	Acknowledgment - Input latch 1 to 8	USINT			•	
		QuitInputLatch01	Bit 0				
		...	...				
		QuitInputLatch08	Bit 7				
4	-	Counter01	UINT	•			
6	-	Counter02	UINT	•			
20	-	Reset counter 1	USINT			•	
		ResetCounter01	Bit 5				
22	-	Reset counter 2	USINT			•	
		ResetCounter02	Bit 5				
8192	-	asy_ModulID	UINT		•		
8196	-	asy_SupplyStatus	USINT		•		
8208	-	asy_SupplyInput	USINT		•		

1) The offset specifies the position of the register within the CAN object.

12.4.1 CAN I/O bus controller

The module occupies 1 digital logical slot on CAN-I/O 1.

12.5 Configuration

12.5.1 I/O mask 1 to 8

Name:
ConfigIOMask01

Channels are configured as inputs/outputs in this register. It also determines whether output monitoring or filtering is applied to the channels. Outputs are monitored but not filtered.

> **Information:**
>
> **In counter operation, channels 1 to 4 can only be configured as inputs.**

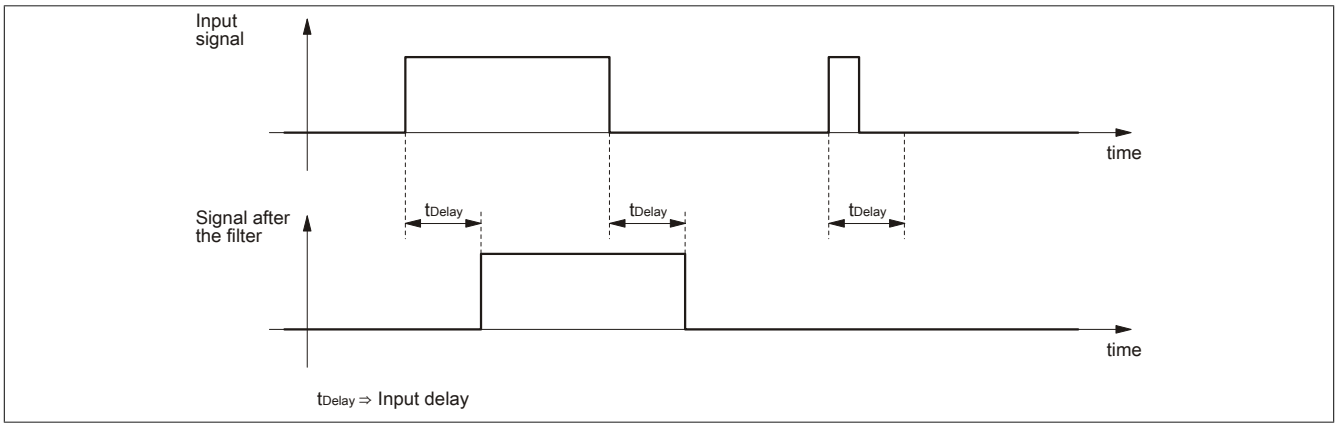
Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Channel 1 configured as input/output	0	Configured as input
		1	Configured as output
...		...	
7	Channel 8 configured as input/output	0	Configured as input
		1	Configured as output

12.5.2 Input filter

An input filter is available for each input. The input delay can be set using register ConfigOutput03. Disturbance pulses which are shorter than the input delay are suppressed by the input filter.



12.5.2.1 Digital input filter

Name:
ConfigOutput03

This register can be used to specify the filter value for all digital inputs.

The filter value can be configured in steps of 100 µs. It makes sense to enter values in steps of 2, however, since the input signals are sampled every 200 µs.

Data type	Value	Filter
USINT	0	No software filter
	2	0.2 ms
	...	...
	250	25 ms - Higher values are limited to this value

12.5.3 Configuration of Counter Channels 1 and 2

Name:
ConfigOutput01 to ConfigOutput02
ResetCounter01 to ResetCounter02

Counter channels 1 and 2 are configured in this register.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0 - 2	Configuration of the counter frequency (only with gate measurement)	000	Counter frequency = 48 MHz
		001	Counter frequency = 3 MHz
		010	Counter frequency = 187.5 kHz
		011 to 111	Reserved
3 - 4	Reserved	0	
5	ResetCounter0x	0	No influence on the counter
		1	Delete counter
6 - 7	Configuration of the operating mode	0	Event counter operation
		1	Gate measurement

Event counter operation

The falling edges are registered on the counter input.

The counter status is collected with a fixed offset to the network cycle and transferred in the same cycle.

Gate measurement

Information:

Only one of the counter channels at a time can be used for gate measurement.

The time of rising to falling edges for the gate input is registered using an internal frequency. The result is checked for overflow (0xFFFF).

The recovery time between measurements must be >100 µs.

The measurement result is transferred with the falling edge to the result memory.

12.6 Communication

12.6.1 Digital inputs

Unfiltered

The input state is collected with a fixed offset to the network cycle and transferred in the same cycle.

Filtered

The filtered status is collected with a fixed offset to the network cycle and transferred in the same cycle. Filtering takes place asynchronously to the network in multiples of 200 µs with a network-related jitter of up to 50 µs.

12.6.1.1 Input state of digital inputs 1 to 8

Name:
DigitalInput01 to DigitalInput08

This register indicates the input state of digital inputs 1 to 8.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalInput01	0 or 1	Input state - Digital input 1
...		...	
7	DigitalInput08	0 or 1	Input state - Digital input 8

12.6.2 Digital outputs

The output status is transferred to the output channels with a fixed offset in relation to the network cycle (SyncOut).

12.6.2.1 Switching state of digital outputs 1 to 8

Name:
DigitalOutput01 to DigitalOutput08

This register is used to store the switching state of digital outputs 1 to 8.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	DigitalOutput01	0	Digital output 01 reset
		1	Digital output 01 set
...		...	
7	DigitalOutput08	0	Digital output 08 reset
		1	Digital output 08 set

12.6.3 Monitoring status of the digital outputs

On the module, the output states of the outputs are compared to the target states. The control of the output driver is used for the target state.

A change in the output state resets monitoring for that output. The status of each individual channel can be read. A change in the monitoring status generates an error message.

12.6.3.1 Status of digital outputs 1 to 8

Name:
StatusDigitalOutput01 to StatusDigitalOutput08

This register is used to indicate the status of digital outputs 1 to 8.

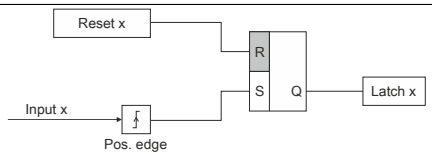
Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	StatusDigitalOutput01	0	Channel 01: No error
		1	Channel 01: Short circuit or overload
...		...	
7	StatusDigitalOutput08	0	Channel 08: No error
		1	Channel 08: Short circuit or overload

12.6.4 Input latch

It works in the same way as a dominant reset RS flip-flop.



R	S	Q	State
0	0	x	Do not change
0	1	1	Set
1	0	0	Reset
1	1	0	Reset

12.6.4.1 Input latch - Rising edges 1 to 8

Name:
InputLatch01 to InputLatch08

The rising edges of the input signal can be latched with a resolution of 200 µs in this register. The input latch is either reset or prevented from latching with register QuitInputLatch0x.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	InputLatch01	0	Do not latch input 1
		1	Latch input 1
...		...	
7	InputLatch08	0	Do not latch input 8
		1	Latch input 8

12.6.4.2 Acknowledgment - Input latch 1 to 8

Name:
QuitInputLatch01 to QuitInputLatch08

This register is used to reset the input latch by channel.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Name	Value	Information
0	QuitInputLatch01	0	Do not reset input 1
		1	Reset input 1
...		...	
7	QuitInputLatch08	0	Do not reset input 8
		1	Reset input 8

12.6.5 Event counter / Gate measurement

Name:
Counter01 and Counter02

Depending on the mode, this register contains the counter value or gate time of channel 1 and channel 2.

Data type	Value
UINT	0 to 65535

12.6.6 Reading the module ID

Name:
asy_ModulID

This register offers the possibility to read the module ID.

Data type	Value
UINT	Module ID

12.6.7 Operating limit status registers

Name:
asy_SupplyStatus

This register can be used to read the status of the operating limits.

Data type	Value
USINT	See bit structure.

Bit structure:

Bit	Description	Value	Information
0	Module power supply within / outside of the warning limits	0	Within the warning limits (18 to 30 V)
		1	Outside of the warning limits (<18 V or >30 V)
1 - 7	Reserved	0	

12.6.8 Module power supply voltage

Name:
asy_SupplyInput

This register contains the module power supply voltage measured by the module.

Data type	Value	Information
USINT	0 to 255	Resolution 1 V

12.6.9 Output supply voltage

Name:
asy_SupplyOutput

This register contains the output supply voltage measured by the module.

Data type	Value	Information
USINT	0 to 255	Resolution 1 V

12.7 Minimum cycle time

The minimum cycle time defines how far the bus cycle can be reduced without communication errors occurring. Note that very fast cycles decrease the idle time available for handling monitoring, diagnostics and acyclic commands.

	Minimum cycle time
Without filtering	150 µs
With filtering	200 µs
Counter operation	250 µs

12.8 Minimum I/O update time

The minimum I/O update time defines how far the bus cycle can be reduced while still allowing an I/O update to take place in each cycle.

	Minimum I/O update time
Without filtering	150 µs
With filtering	200 µs
Counter operation	250 µs